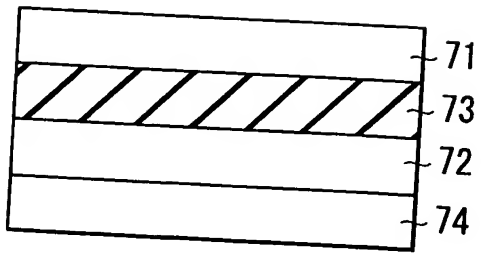


FIG. 1

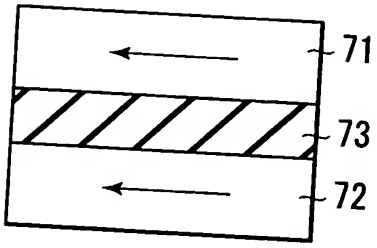


FIG. 2A

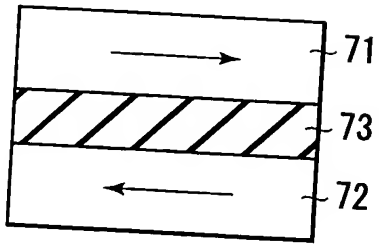


FIG. 2B

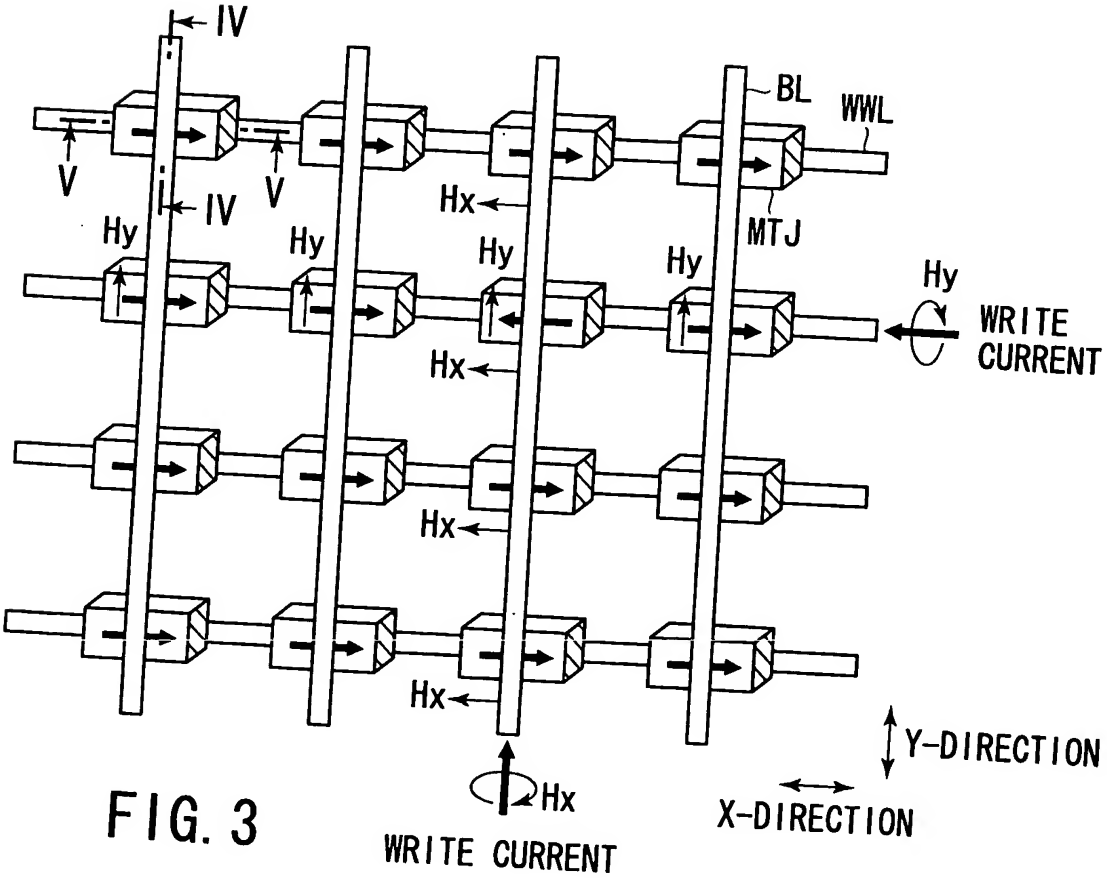


FIG. 3

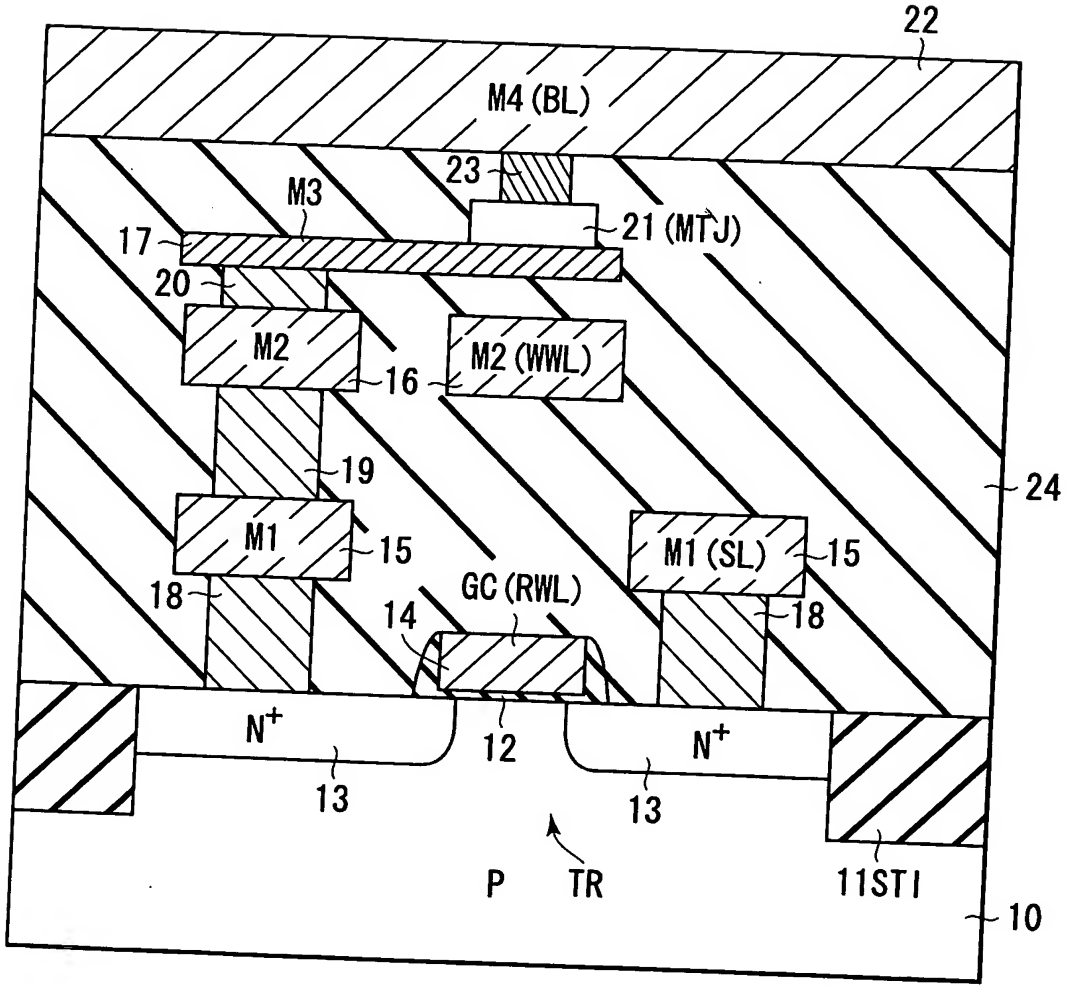

22
M4 (BL)
23
M3
21 (MTJ)
17
20
M2
16
M2 (WWL)
19
24
M1
15
M1 (SL)
15
18
GC (RWL)
14
18
N+
12
N+
13
13
P
TR
11STI
10

FIG. 4

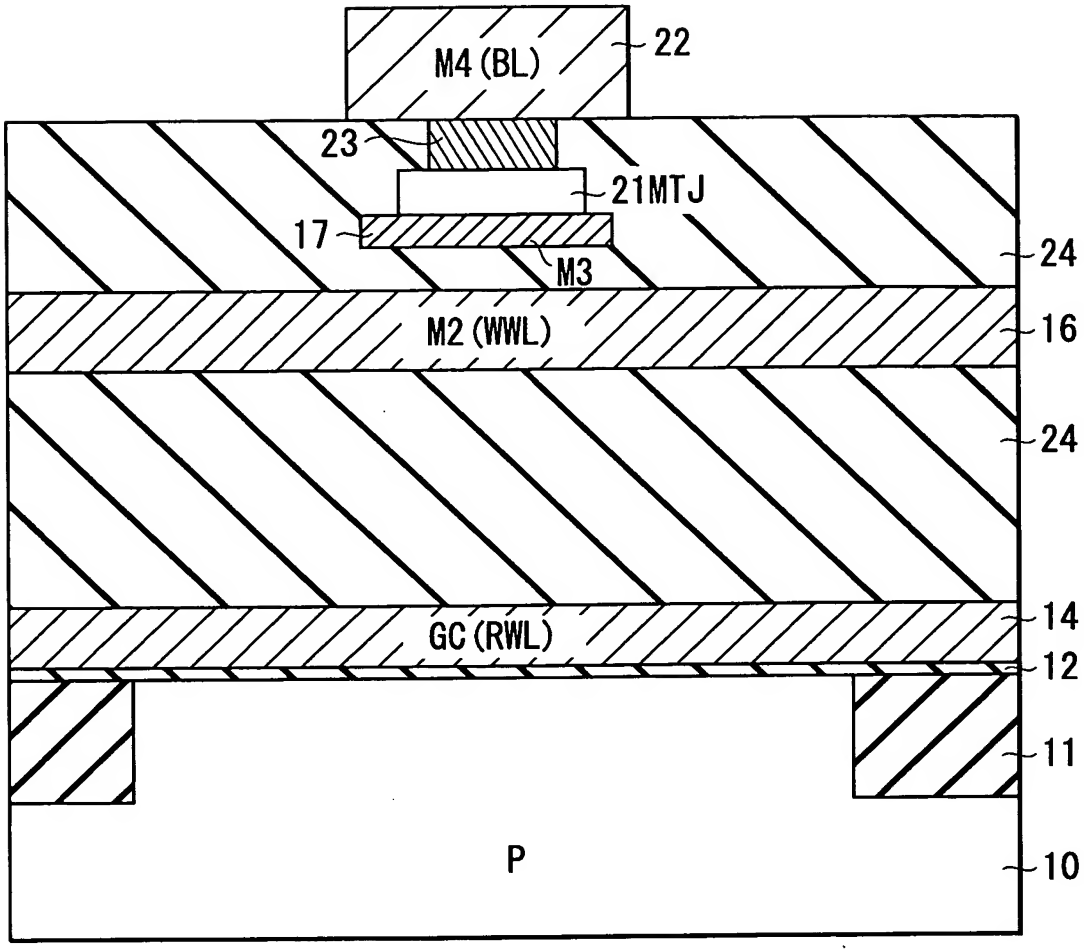

M4 (BL)
22
23
21MTJ
17
M3
24
M2 (WWL)
16
24
GC (RWL)
14
12
11
P
10

FIG. 5

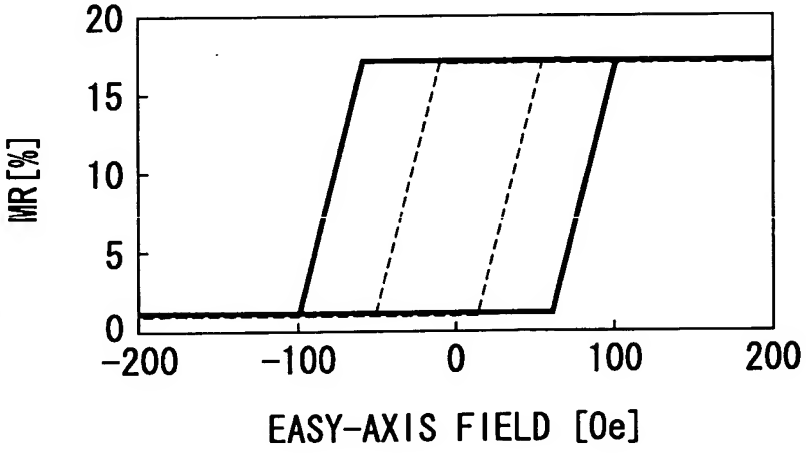

20
15
10
5
0
MR [%]
-200
-100
0
100
200
EASY-AXIS FIELD [Oe]

FIG. 6

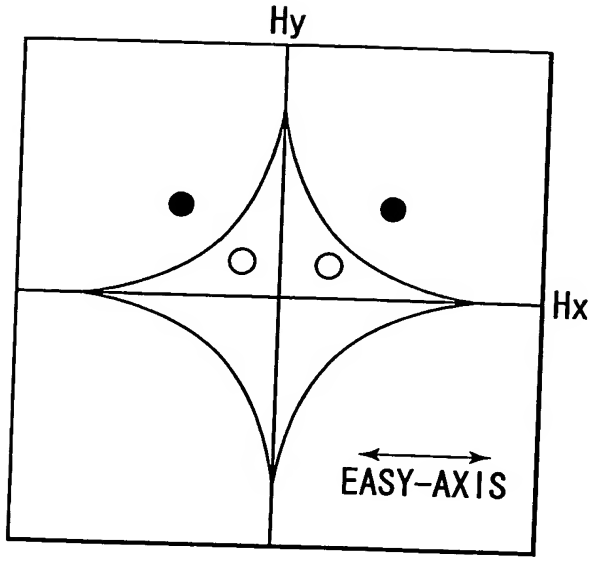

Hy
Hx
EASY-AXIS

FIG. 7

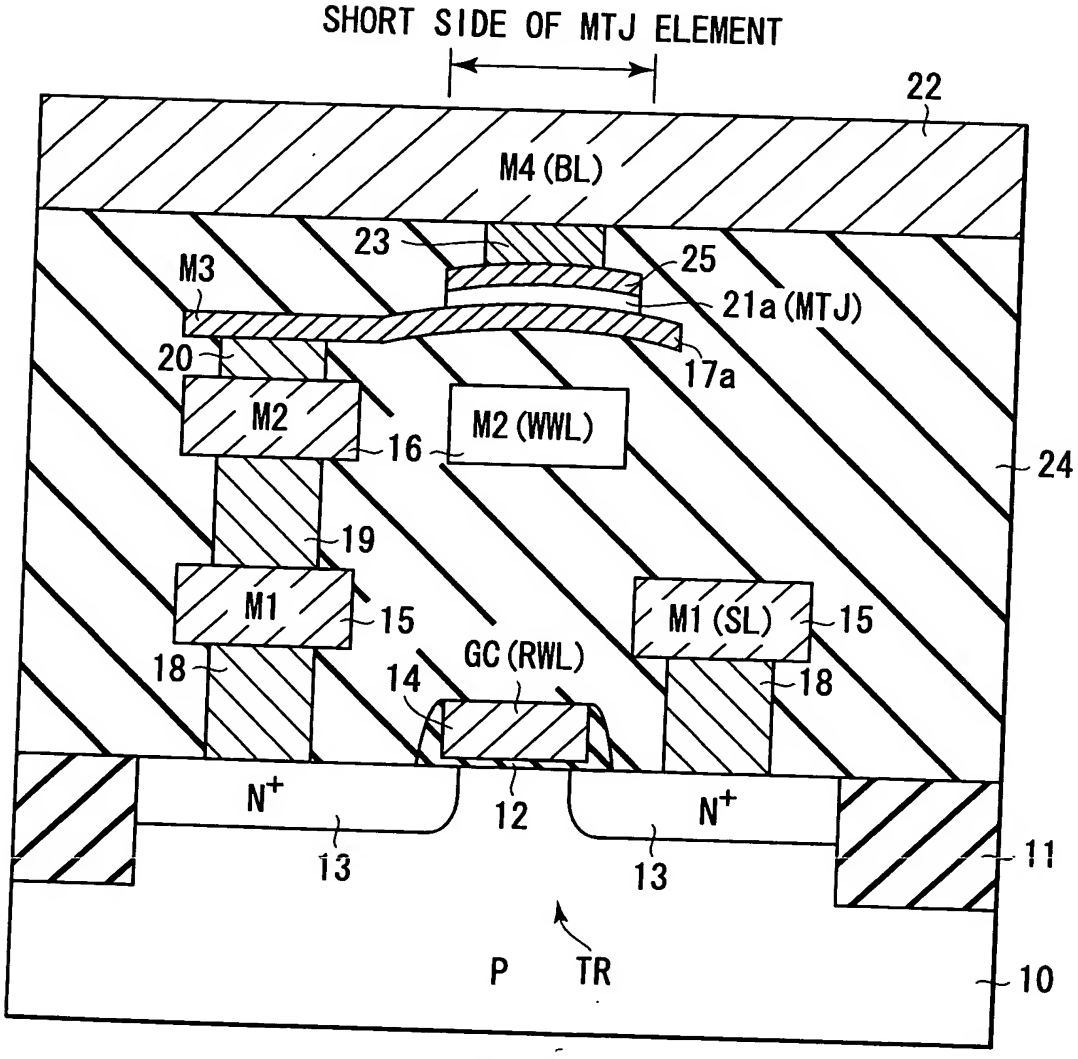

SHORT SIDE OF MTJ ELEMENT
22
M4 (BL)
23
25
M3
21a (MTJ)
20
17a
M2
M2 (WWL)
16
24
19
M1
15
M1 (SL)
15
18
GC (RWL)
14
18
N+
12
N+
13
13
11
P
TR
10

FIG. 8

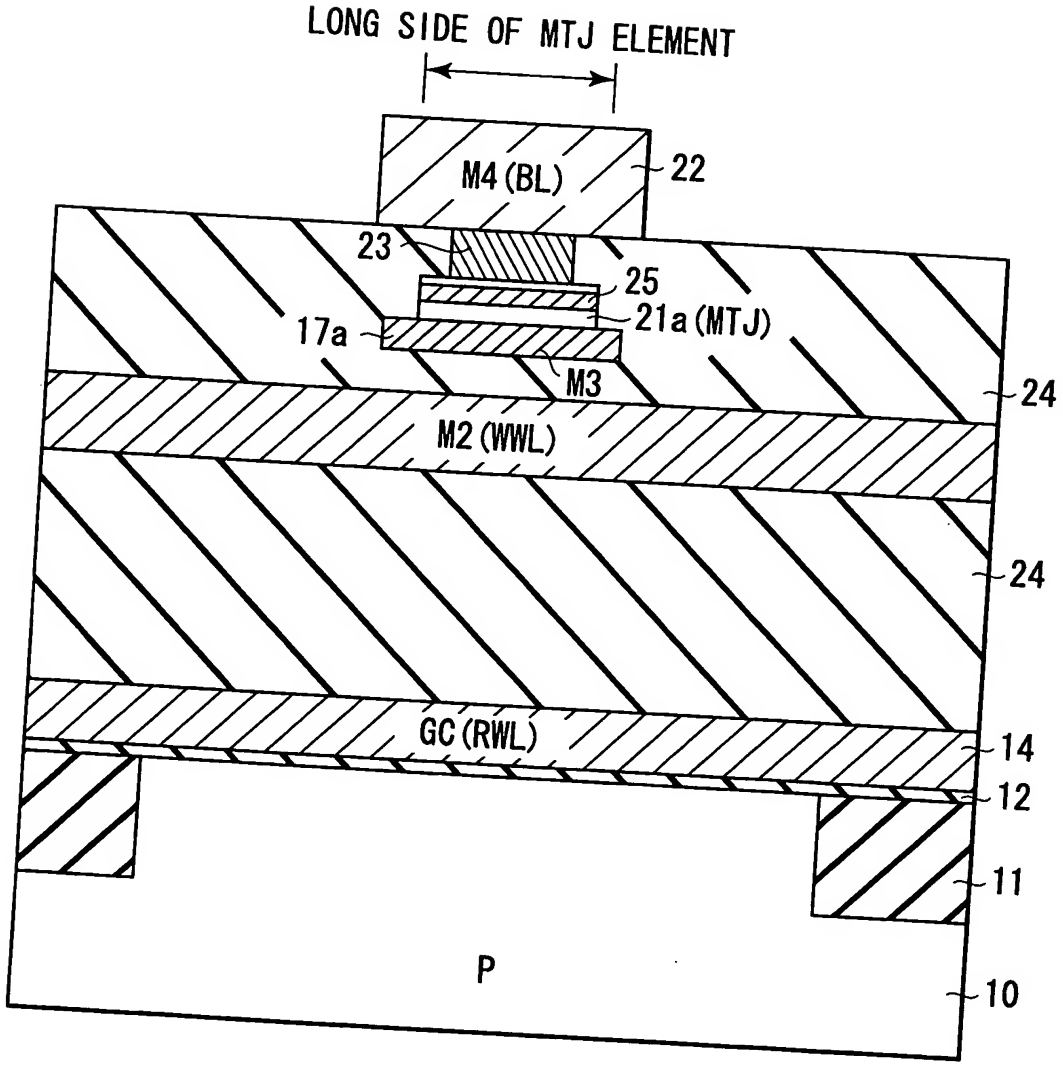

LONG SIDE OF MTJ ELEMENT
M4 (BL)
22
23
25
21a (MTJ)
17a
M3
24
M2 (WWL)
24
GC (RWL)
14
12
11
P
10

FIG. 9

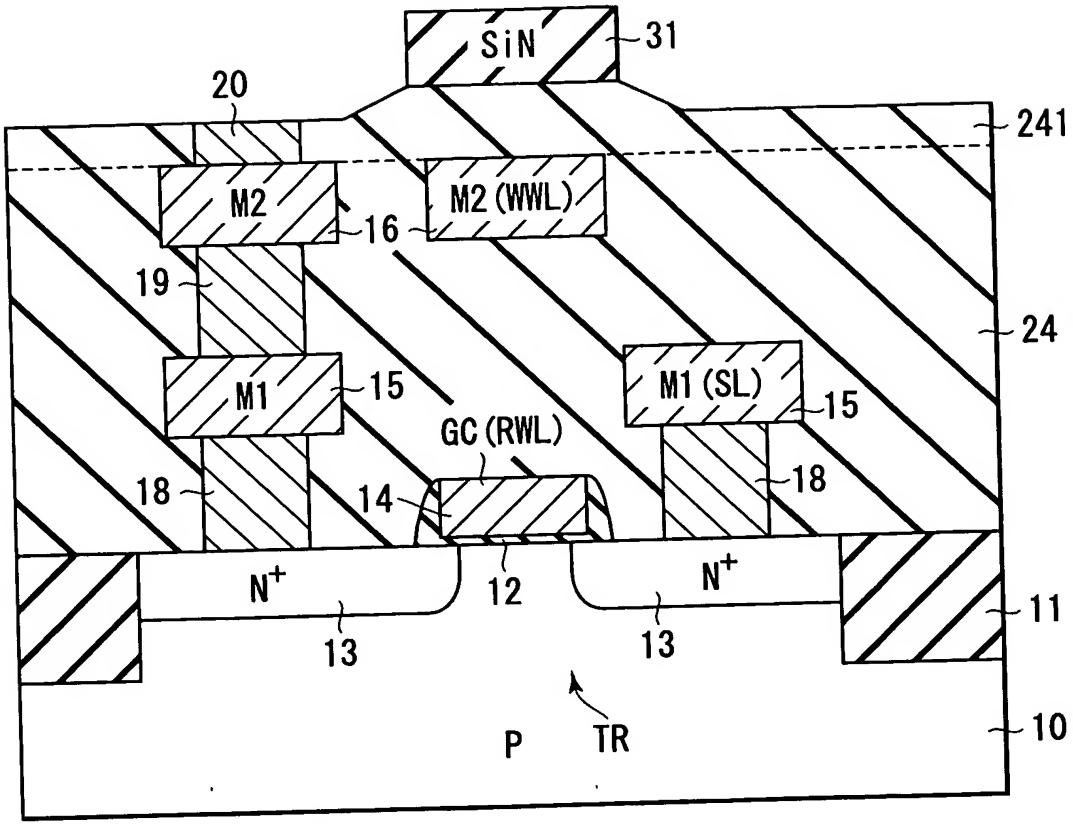

SiN
31
20
241
M2
M2 (WWL)
16
19
24
M1
15
M1 (SL)
15
GC (RWL)
18
14
18
N+
12
N+
13
13
11
P
TR
10

FIG. 10

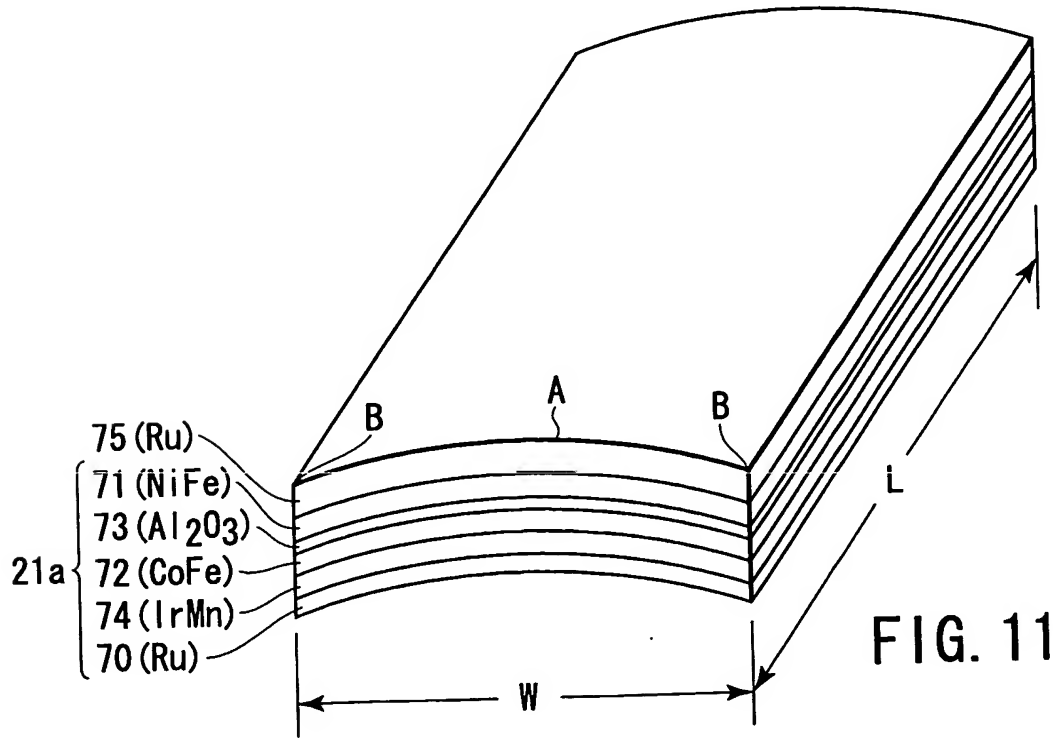

75 (Ru)
71 (NiFe)
73 (Al2O3)
21a
72 (CoFe)
74 (IrMn)
70 (Ru)
B
A
B
L
W

FIG. 11

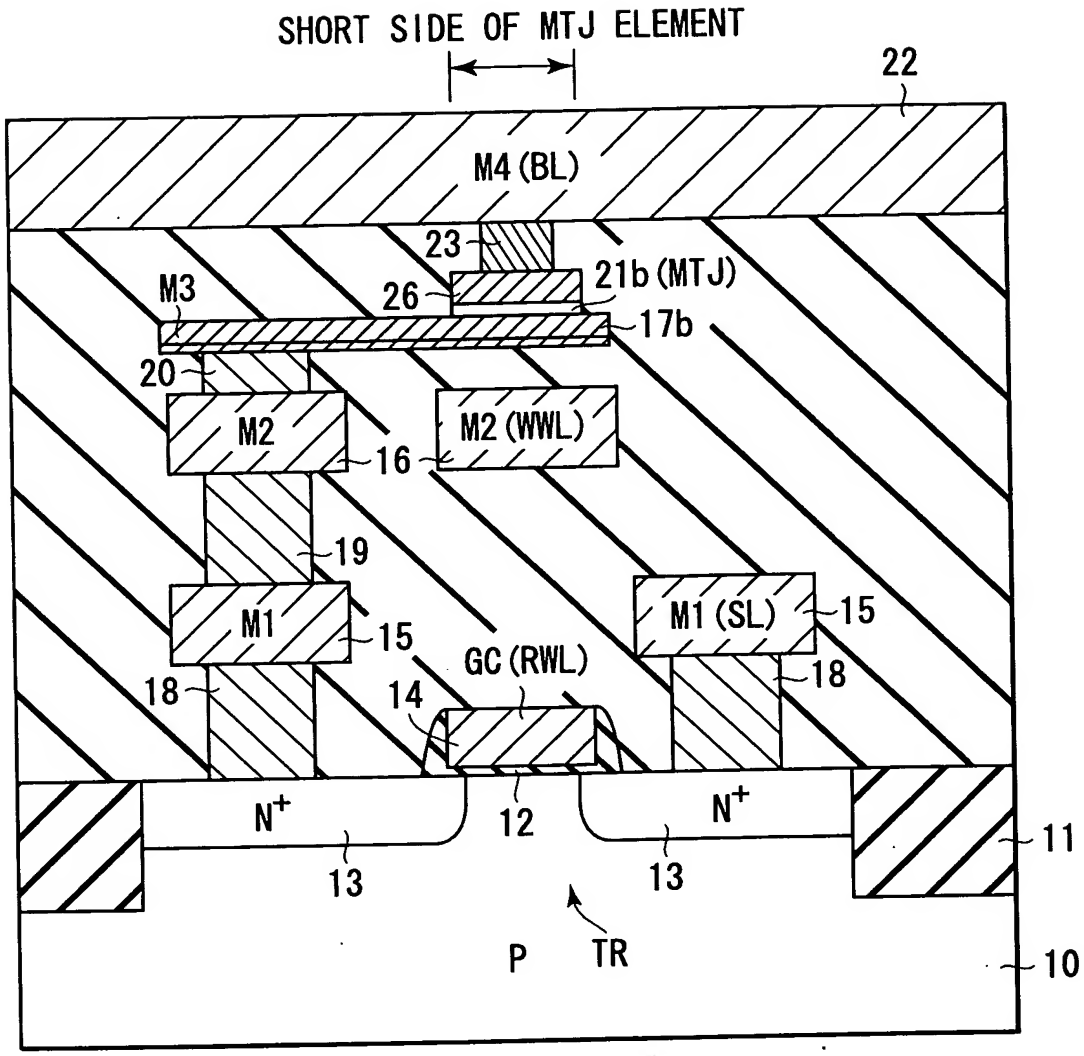

SHORT SIDE OF MTJ ELEMENT
22
M4 (BL)
23
21b (MTJ)
26
M3
17b
20
M2
M2 (WWL)
16
19
M1
15
M1 (SL)
15
GC (RWL)
18
14
18
N+
12
N+
11
13
13
P
TR
10

FIG. 12

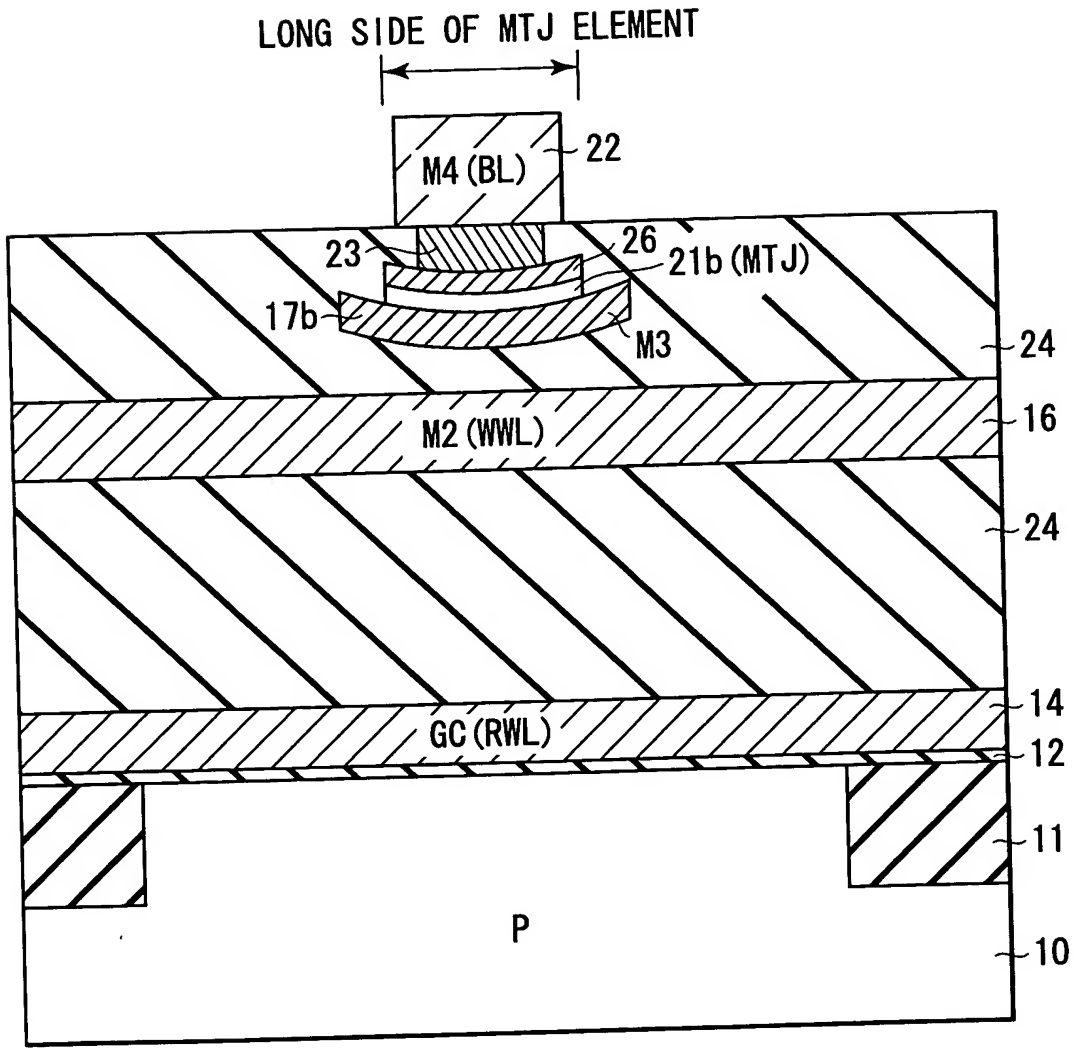

LONG SIDE OF MTJ ELEMENT
M4 (BL)
22
23
26
21b (MTJ)
17b
M3
24
M2 (WWL)
16
24
14
GC (RWL)
12
11
P
10

FIG. 13

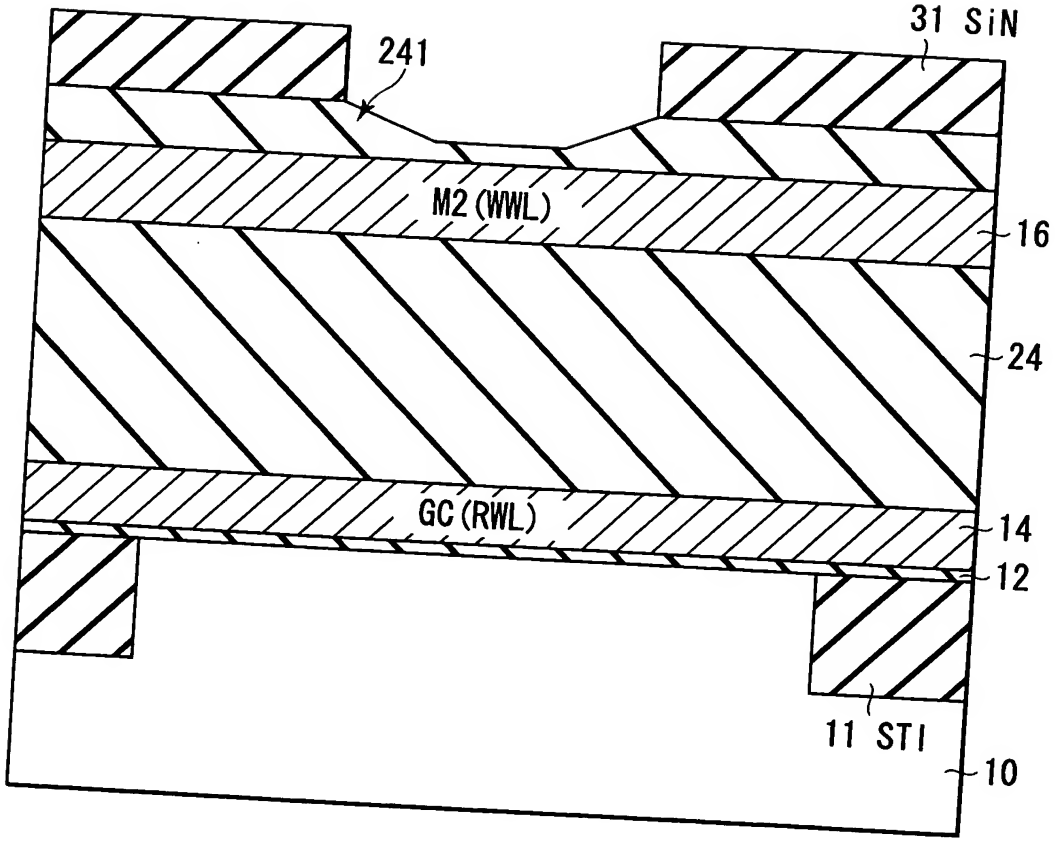


FIG. 14

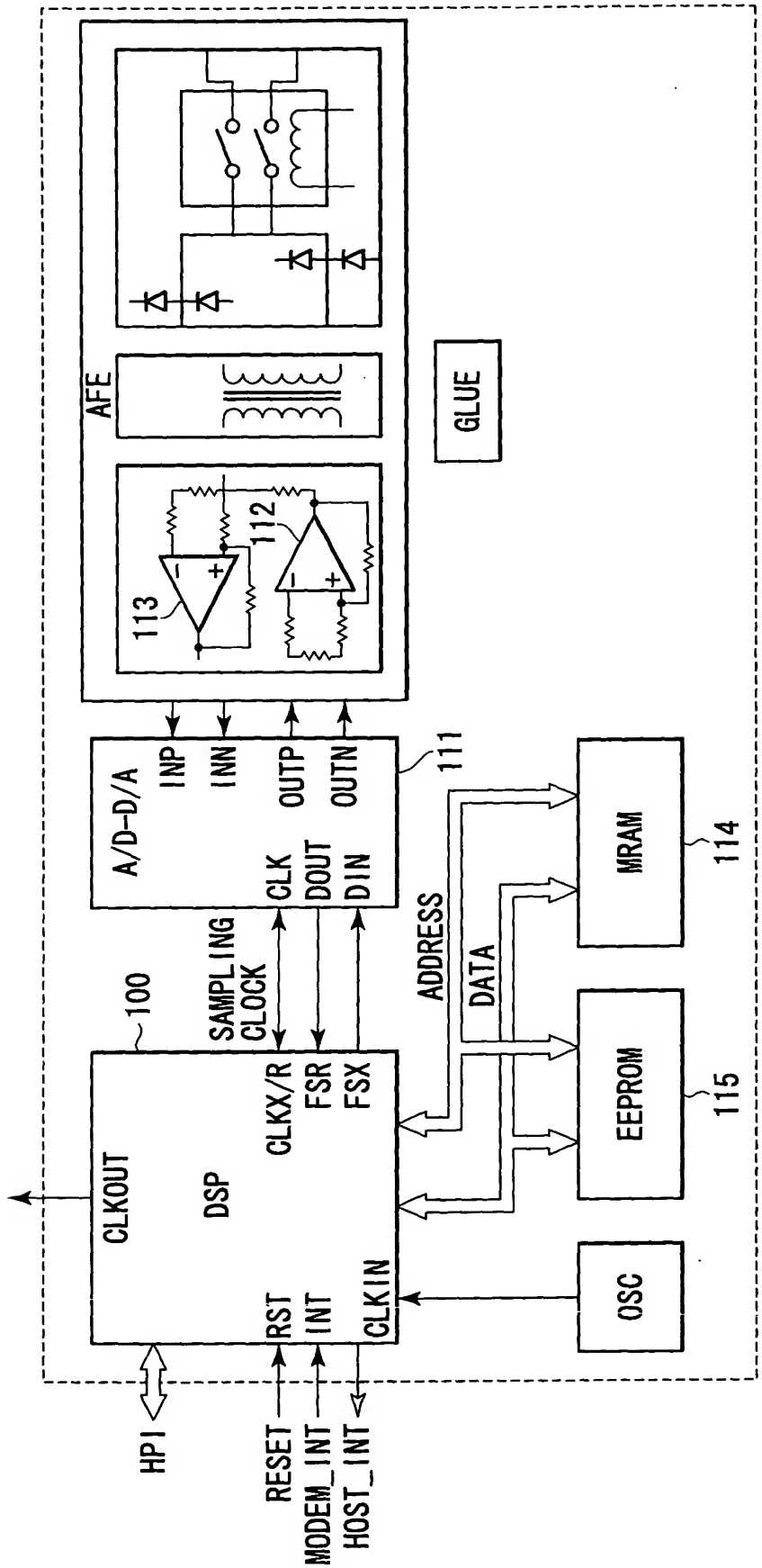

AFE
GLUE
113
112
A/D-D/A
INP
INN
OUTP
OUTN
111
CLK
DOUT
DIN
SAMPLING CLOCK
100
ADDRESS
DATA
MRAM
114
CLKOUT
DSP
CLKX/R
FSR
FSX
EEPROM
115
OSC
RST
INT
CLKIN
HPI
RESET
MODEM_INT
HOST_INT

FIG. 15

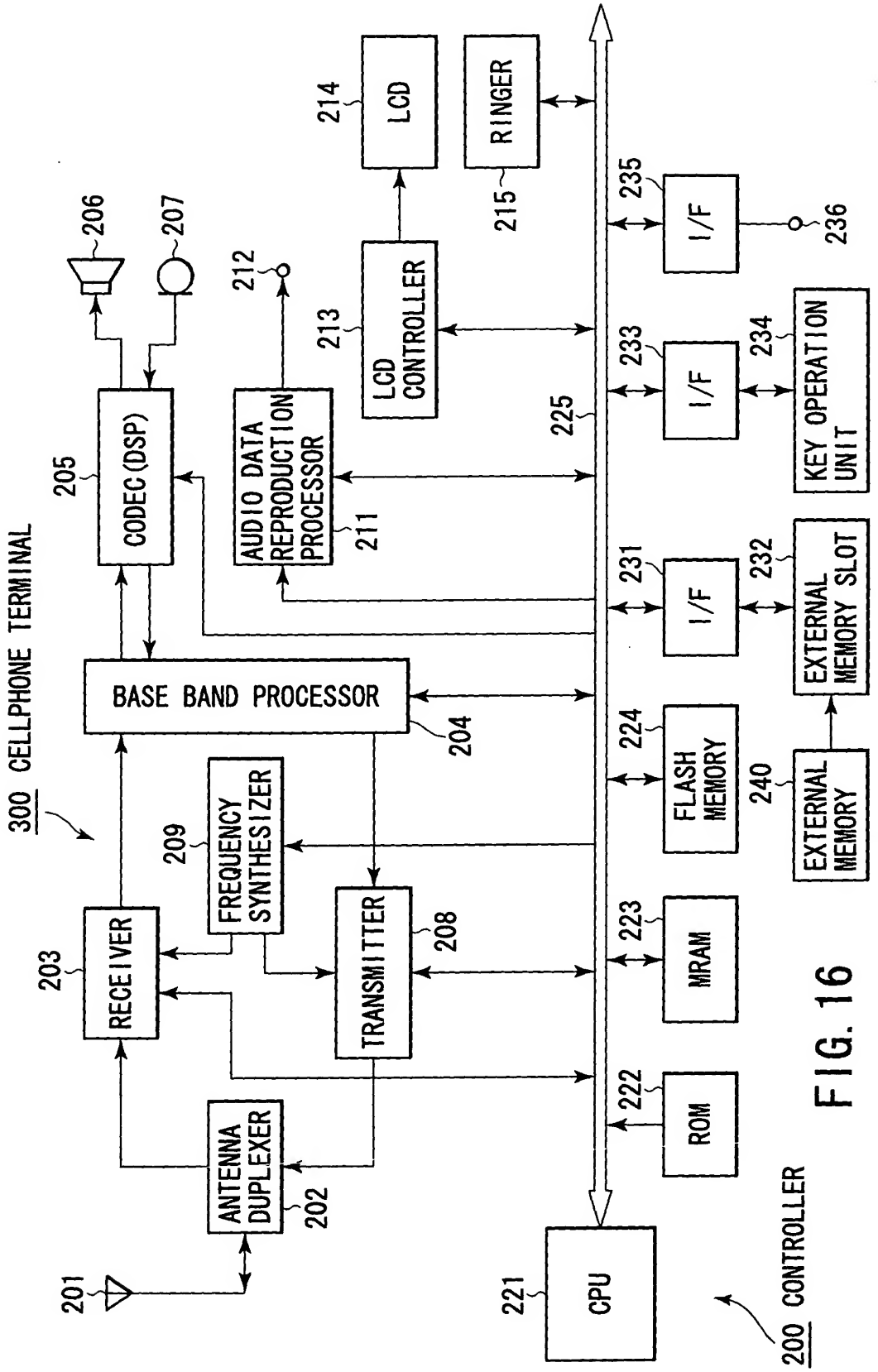

300 CELLPHONE TERMINAL
200 CONTROLLER
201
202
ANTENNA DUPLEXER
203
RECEIVER
204
BASE BAND PROCESSOR
205
CODEC (DSP)
206
207
208
TRANSMITTER
209
FREQUENCY SYNTHESIZER
211
AUDIO DATA REPRODUCTION PROCESSOR
212
213
LCD CONTROLLER
214
LCD
215
RINGER
221
CPU
222
ROM
223
MRAM
224
FLASH MEMORY
225
231
I/F
232
EXTERNAL MEMORY SLOT
233
I/F
234
KEY OPERATION UNIT
235
I/F
236
240
EXTERNAL MEMORY

FIG. 16

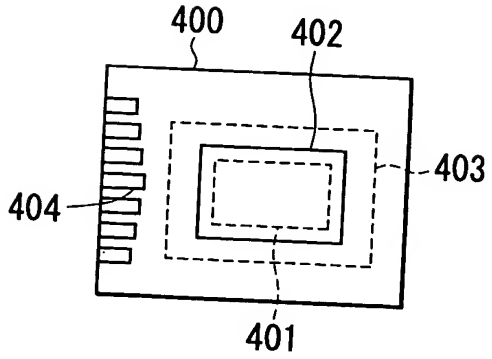


FIG. 17

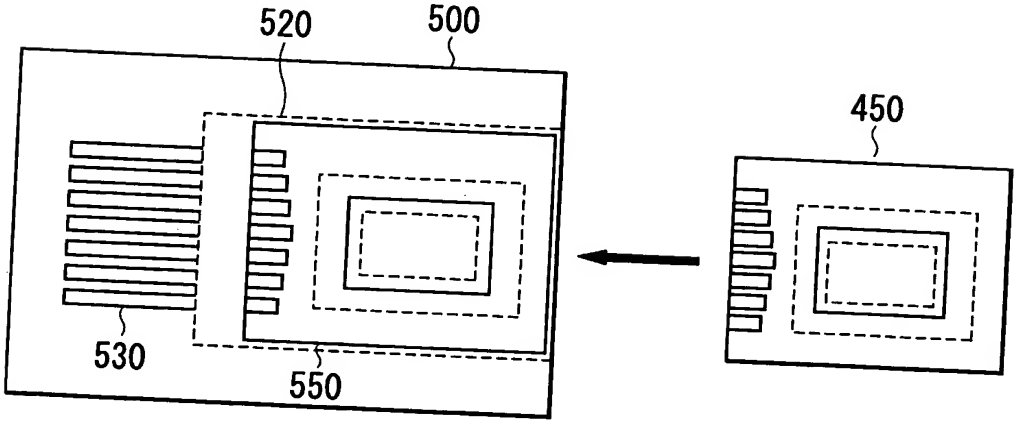
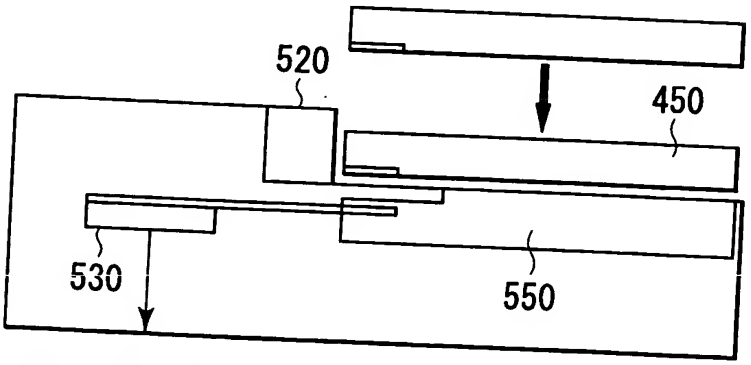


FIG. 18



TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 20

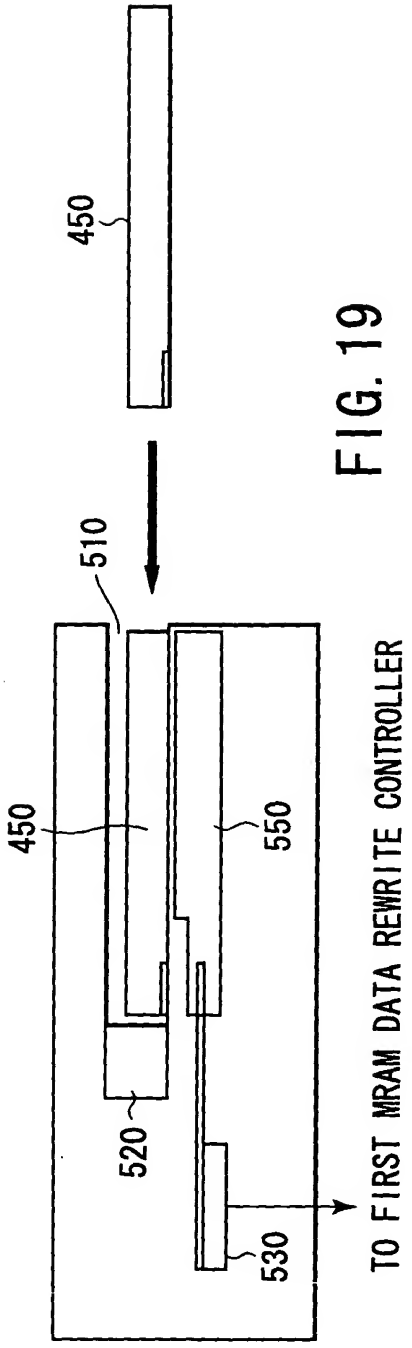

450
510
450
550
520
530
TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 19

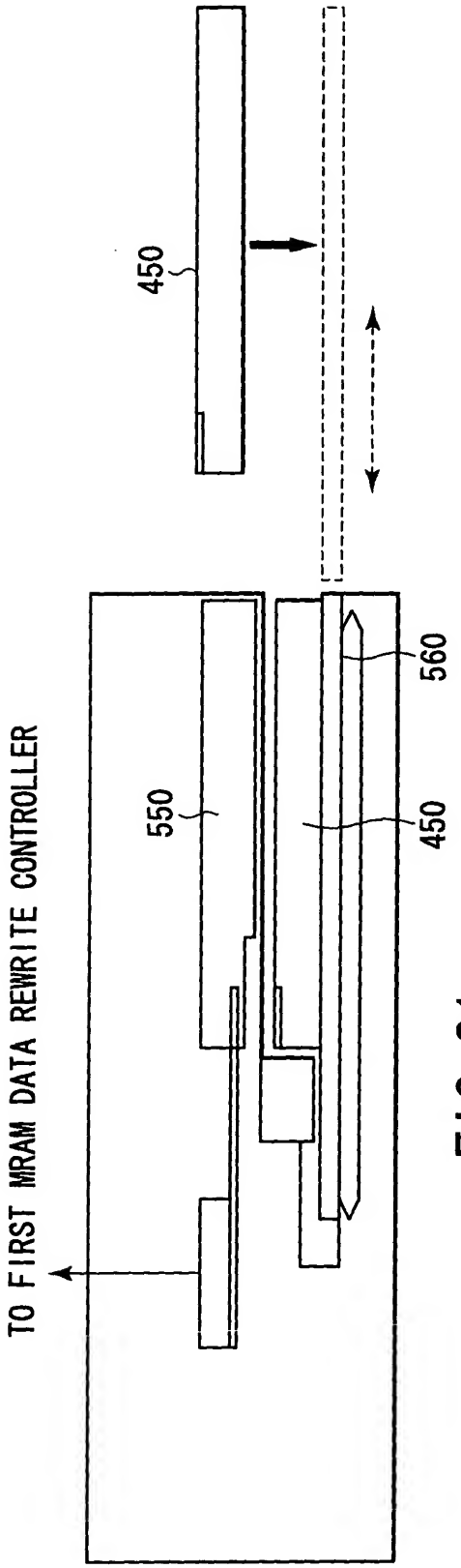

450
560
550
450
TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 21